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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/733,254 | 12/08/2000 | Elana D. Granston | TI-29189 | 3119 |

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| EXAMINER | |
|---|---|
| VU, TUAN A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2124 | 2 |

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/733,254 | GRANSTON ET AL. | |
| | Examiner | Art Unit | |
| | Tuan A Vu | 2124 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *08 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/08/2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is responsive to the application filed December 8, 2000.

Claims 1-6 have been submitted for examination.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the register" in "copying back to the register" ( line 11). There is insufficient antecedent basis for this limitation in the claim. The examiner would interpret this 'register' as if it were the active or original register to proceed on with the examination.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rau et al., "Code Generation Schema for Modulo Scheduled Loops", ACM Proceedings of the 25th annual International Symposium on Microarchitecture, Dec 1992, volume 23, iss. 1-2, (hereinafter Rau_1), in view of Rau et al., "Register Allocation for Software Pipelined Loops", June 1992, In

Proc. of the ACM SIGPLAN'92 Conference on Programming Language Design and Implementation, pages 283-299 ( hereinafter Rau_2), and further in view of Akkary, USPN: 6,240,509 ( hereinafter Akkary).

**As per claim 1**, Rau_1 discloses a method for pipelining program loops having irregular loop control comprises the steps of:

determining which instructions in loop code in a memory may be speculatively executed (e.g. pg. 161, ch.2.3; pg. 163, ch. 3.1, 3.2);

storing in a computer memory a set of registers (e.g. pg. 161, ch. 2.1; *rotating registers* - pg. 164, ch. 3.4; pg. 169, Fig. 9-11);

But Rau does not explicitly disclose storing a set of registers that are modified by an instruction and are alive out of the loop. Rau_2, in a method to support the pipelining of loops and control thereof, discloses the use of rotating registers analogous to Rau_1 and further provides keeping of registers that are modified by an instruction and alive out of the loop iteration ( e.g. *register allocator , loop-variant, virtual register, live-in, live-out, scalar lifetime, vector lifetime* - pg. 284-286, ch. 1.3 – Note: the allocation of register in conjunction with determining of loop related variants is equivalent to storing registers modifiable by loop instructions). It would have been obvious for one of ordinary skill in the art at the time the invention was made to provide the loop-related live register monitoring or recording as taught by Rau_2, in case Rau_1 does not already include one such process, because this would enable the allocation of registers more effective and more resource-focused in keeping pace with variables being changed as a result of a loop iteration or pipeline kernel/stage completion.

Nor does Rau_1 disclose modifying the program code so that the values of those registers are saved to a temporary register during all proper iterations; and copying back to the register the value of the temporary register once the loop is completed. Rau_1, however teaches the execution of code based on speculated execution and predicated execution via use of special instructions and registers (e.g. pg. 164, cha.p 3.4, 3.5) hence suggests means to optimize register resources usage ( e.g. pg. 168-169, Fig. 7-10), to address the temporal effects or overlapping usage of values fetched in different stages of iterations and/or overlapped loops execution. In a method using speculation in handling pipelined loops analogous to that of Rau_1, Akkary discloses the use of temporary registers and instruction trace buffer for execution of the speculation-intensive pipeline in order to prevent mis-speculation recovery resources (e.g. Fig. 12-16; col. 11, line 60 to col. 12, line 22); hence teaches the committing or copying of values from the temporary registers to the original active registers used in the execution. It would have been obvious for one of ordinary skill in the art at the time the invention was made to add to the register allocation by Rau_1 ( enhanced by Rau_2) the use of hardware support such as temporary registers as taught by Akkary, because this would allow variants from overlapping stages of pipelined loops execution to be maintained prior to being committed or copied back to the virtual registers before the next loop iteration is undertaken, so to make optimal use of registers resources as intended by both Rau_1 and Rau_2.

**As per claim 2 and 3**, Rau_1 teaches minimizing the latency due to initiation interval between iterations, applying the optimization with intent reduce to kernel-only pipelines ( e.g. pg. 158-160; *kernel-only* – pg. 164, ch. 3.5), hence has implicitly disclosed downsizing to loop pipelining ( re claim 2) with a minimum trip count being reduced to 1; further, Rau_1 discloses

one structure pipeline of loop to which modulo schedules is applied (e.g. pg. 158-160), hence has implicitly disclosed elimination ( re claim 3) of multi-version loop code.

**As per claim 4**, Rau_1 discloses a method for software pipelining of irregular conditional control loops, the method including pre-processing the loops so they can be safely pipelined, comprising:

pre-processing each instruction in the loop in turn (e.g. *loop-variant, basic block , unrolling, modulo scheduling* -- pg. 158-159, ch. 1.2);

if the instruction can be safely speculated, leaving it alone (e.g. pg. 163-164, ch. 3.1, 3.2 – Note: speculation can be executed without additional need to set up for predicated instruction is equivalent to let speculative execution alone);

pre-processing the instruction using predication (e.g. pg. 161, ch. 2.2; pg. 164, ch. 3.4-3.5 – Note: predication such as If-conversion using control register implicitly discloses an alternate means to using speculative execution because the former requires additional setting resources compared to the latter).

But Rau_1 does not explicitly disclose pre-processing of instructions that modify registers that are live out of the loop. But Rau_1 teaches register use for iteration control ( pg. 161, ch. 2.1-2.2) hence has implicitly taught a certain level of instruction analysis in conjunction with modifying contents of a register. The limitation as to use analysis on alive register out of a loop has been addressed in claim 1 using Rau_2 using the rationale that analyzing of live registers would enhance the saving of resources while allocating of registers during the process of minimizing resources reuse and variables overlapping across iterations of pipelined loops.

Nor does Rau_1 disclose register copying upon determining that an instruction modifies registers as seen above. But this limitation as to use temporary storage such as buffers and registers for later recopying usable value in the original active register has been addressed using the teachings by Akkary in claim 1 above, and is rejected herein using the corresponding rationale.

**As per claim 5**, the alternate use of predication execution to the speculative execution has been addressed in claim 4 above, using Rau_1.

**As per claim 6**, Rau_1 discloses speculatively executing of instructions but fails to disclose that such execution is due to modifying of registers that are live out of the loop; but this missing limitation has been obviated using Rau_2' teachings as mentioned in claim 4 or 1 above.

Nor does Rau_1 disclose pre-processing using register copying; but this also has been addressed in claim 4 and 1 above.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat No. 5,930,492 to Lynch, disclosing temporary registers for use in code insertions in pipelines.

Schlansker et al., "Achieving High Levels of Instructions-Level Parallelism with Reduced Hardware Complexity", Nov 1994, HPL-96-120, www.hpl.hp.com/techreports/96/HPL-96-120.pdf, disclosing modulo scheduling with speculation of branch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

**Any response to this action should be mailed to**:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

(703) 872-9306 ( for formal communications intended for entry)

**or:** (703) 746-8734 ( for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor( Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
October 15, 2003

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100